

**II.B.TECH- I-SEM -II MID EXAMINATIONS *Date:*  02.12.2024 Time*: 01.30PM-03.30PM***

**Subject: ADE Branch: IT Marks: 30M**

**Note: Question paper contains two parts, Part - A and Part - B.**

**Part-A is compulsory which carries 10 marks. Answer all questions in part-A.**

**Part-B consists of (2 1/2) units. Answer any one full question from each unit. Each question carries 5 marks and may have a,b,c sub questions.**

# PART-A 5x2=10

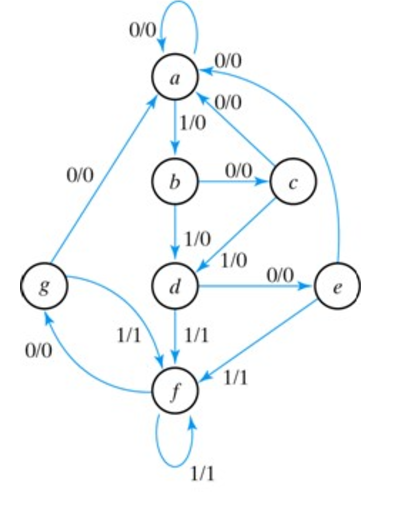
1. What is the purpose of Multiplexer? Explain about 4x1 MUX.? [BTL-1] [CO-5]
2. Compare synchronous sequential and asynchronous sequential circuits ? [BTL-2] [CO-5]
3. What are universal logic gates? Explain how do you realize an X-OR gate? [BTL-6] [CO-6]
4. Define Logic family and mention various types of it? [BTL-1] [CO-6]
5. Draw the structure of T Flip flop? [BTL-2] [CO-6]

PART-B 4X5=20

1. Obtain the minimal SOP expression for the switching function using k-map

Y=∑ m (0,2,3,6,7) + ∑ d (8,10,11,15),Draw and explain the logic diagram.? [BTL-6] [CO-4]

1. Construct 4-to-2-line Encoder with logic gates and truth table.? [BTL-4] [CO-5]
2. Define shift registers? Explain about the operation of universal shift register [BTL-2] [CO-5]
3. Explain the operation NAND and NOR DTL gates? [BTL-3] [CO-6]
4. Explain about Synchronous Counter in detail. [BTL-3] [CO-5]
5. Reduce the given state diagram. [BTL-5] [CO-5]



| **Scheme of Evaluation(MID-2)** | | | |
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| **S.No** | **Theory(Part-A)** | **Marks** | **Total** |
| 1 | Define multiplexer  Draw 4x1 Multiplexer | 1M  1M | **2M** |
| 2 | Any two comparision of asychronous and synchronous sequential circuits | 2M | **2M** |
| 3 | Define universal logic gates  Draw X-OR circuit with universal logic gates | 1M  1M | **2M** |
| 4 | Define logic family  Mentioned types | 1M  1M | **2M** |
| 5 | Draw the structure if T flip flop | 2M | **2M** |
| **Total** | | | **10M** |

| **S.No** | **Theory(Part-B)** | **Marks** | **Total** |
| --- | --- | --- | --- |
| **6** | Minimize the K map with SOP expressions using K map  Draw the logic diagrams | 3M  2 M | **5M** |
| **7** | Definition Encoder,  construct the 4 x 2 encoder with logic gates and truth table | 1 M  4M | **5M** |
| **8** | Definition of shift register  Explanation about the universal Shift Registers | 1M  4M | **5M** |
| **9** | Define DTL gate  Design the NAND and NOR gates using DTL each design carries @2M | 1M  4 M | **5M** |
| **10.** | Defination of synchronous counter  Explanation of synchronous counter | 1 M  4M | **5M** |
| **11.** | State reduction method simplification  Draw the reduced state diagram | 3 M    2M | **5M** |